AMENDMENTS TO THE SPECIFICATION:

Please amend the title as follows:

LOW POWER SEMI-TRACE INSTRUCTION/TRACE HYBRID CACHE WITH LOGIC FOR INDEXING THE TRACE CACHE UNDER CERTAIN CONDITIONS

Please amend paragraph [0015] as follows:

[0015] Again, the TCache portion stores instructions in program order rather than in address order and contains a complete line of usable instructions (in the case of a correct prediction). Thus, the TCache portion is filled with traces gleaned either from the actual stream of retired instructions, or instructions predicted before execution. Note that the TCache portion is only indexed when processor 12 executes certain instructions such as, for example, a branch, a jump, a call, a return, etc. (see Fig. 4). Accordingly, TCache line 210 may contain non-contiguous instructions from an instruction stream having, for example, branches that include instructions that start at a branch target and potentially continue through other taken branches. Consequently, a plurality of instructions including instructions crossing a predicted branch boundary may be fetched from the TCache portion of semi-trace cache 20 with only one address/access. Traces may be built using a line buffer (or fill-unit) that records instructions as they are retired from the execution core and the instructions may be inserted into semi-trace cache 20 when a trace end-condition is encountered.

Please amend paragraph [0018] as follows:

[0018] FIG. 3 is a diagram that illustrates reading from the semi-trace cache and FIG. 4 is a flow diagram 400 that shows functional operation of semi-trace cache 20. As shown in FIG. 4, block 402 shows that an instruction is fetched from the current line of semi-trace cache 20. At block 430, a determination is made whether the instruction is fetched from ICache and is a jump, branch, call, or return instruction. If the conditions of block 430 are met, the TCache portion is indexed with the address of the current instruction at block 431. The~~That~~ fetched instruction is executed by processor 12 as indicated by block 404. At block 432, the current instruction is inserted into semi-trace cache 20 or a line buffer as discussed above. In block 406 a determination is made as to whether the executed instruction causes processor 12 to take a change in the flow-of-control. Different actions may be taken depending on whether processor 12 is running from the TCache portion or the ICache portion. For instance, when running from the TCache portion a change in flow-of-control may occur when a branch is mispredicted or an end of the line is reached. If there is no change in flow, then in block 408, a check is made to determine if the last instruction in the current line was fetched and executed. If the last instruction was not fetched then control is looped back to block 402.